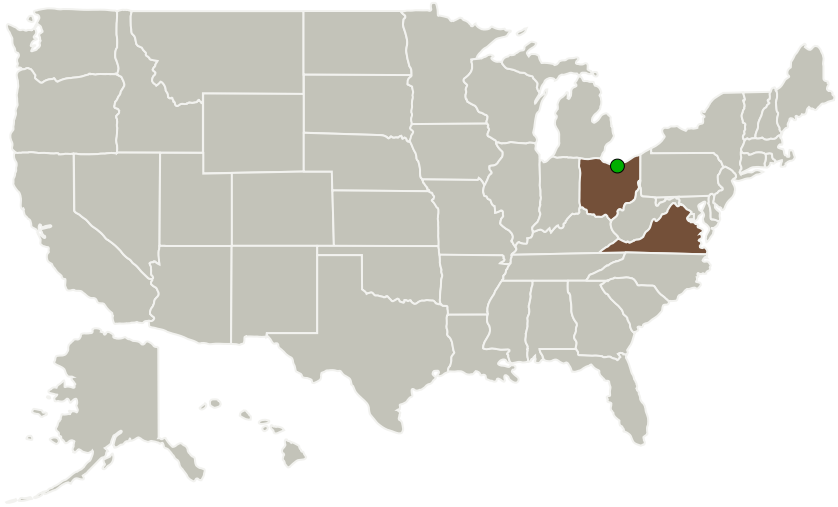
Monolithically Integrated Rad-Hard SiC Gate Driver for 1200 V DMOSFETs, Phase I

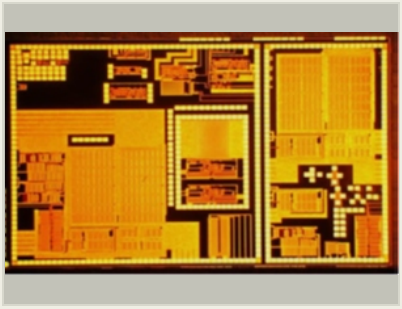
Completed Technology Project (2016 - 2017)

Project Introduction

This two-phase SBIR program targets the need for highly integrated SiC-based electronics systems by developing analog and digital circuits that can be fully integrated with 4H-SiC power switching devices, enabling eventual realization of a monolithic, highly integrated gate driver circuit. Specifically, the final goal of this program is to develop and demonstrate a fully integrated, isolated, high-side/low-side gate driver architecture, having an integrated SiC power MOSFET. In addition to integrated resistors and capacitors, development of SiC CMOS technology will entail the demonstration of lateral SiC NMOSFETs and the more challenging SiC PMOSFET devices with adequate performance and radiation hardness. During Phase I, the development of a rad-hard SiC PMOS process will be investigated. In parallel, capitalizing on GeneSiC's already developed SiC NMOS process, an NMOS-only gate drive buffer circuit will be designed and implemented on the same host substrate as 1200 V SiC DMOSFETs. Compact device models will be generated during Phase II from the results of the SiC NMOS/PMOS process development. Pending successful development of a rad-hard SiC PMOS process during Phase I, Phase II will focus on building an entire SiC CMOS-based gate drive circuit and integrating it with a 1200 V SiC DMOSFET.

Primary U.S. Work Locations and Key Partners





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Organizations Performing Work	Role	Type	Location
GeneSiC Semiconductor Inc.	Lead Organization	Industry Minority-Owned Business, Small Disadvantaged Business (SDB)	Dulles, Virginia
Glenn Research Center(GRC)	Supporting Organization	NASA Center	Cleveland, Ohio

Primary U.S. Work Locations	
Ohio	Virginia

Project Transitions

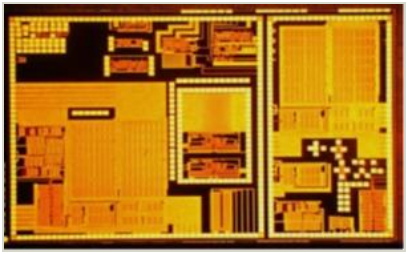
June 2016: Project Start

January 2017: Closed out

Closeout Documentation:

- Final Summary Chart*(https://techport.nasa.gov/file/140213)*

Images



Briefing Chart Image
Monolithically Integrated Rad-Hard SiC Gate Driver for 1200 V DMOSFETs, Phase I
(https://techport.nasa.gov/image/136569)

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

GeneSiC Semiconductor Inc.

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

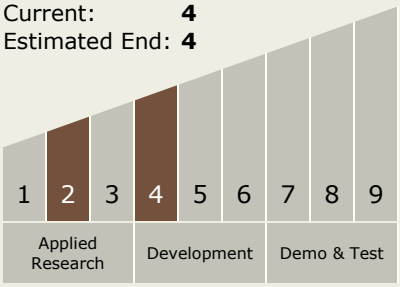
Carlos Torrez

Principal Investigator:

Ranbir Singh

Technology Maturity (TRL)

Start: **2**
Current: **4**
Estimated End: **4**



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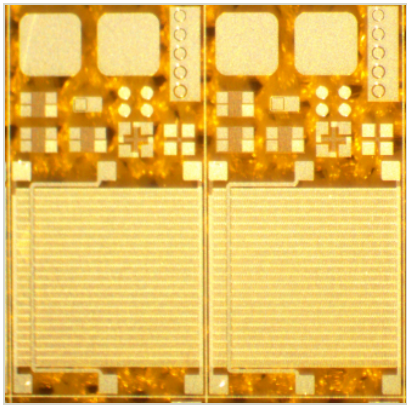

Final Summary Chart Image
Monolithically Integrated Rad-Hard SiC Gate Driver for 1200 V DMOSFETs, Phase I Project Image *(https://techport.nasa.gov/image/132913)*

Technology Areas

Primary:

- TX03 Aerospace Power and Energy Storage
  - TX03.3 Power Management and Distribution
    - TX03.3.3 Electrical Power Conversion and Regulation

Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System